IDEC Chip Design Contest

A 20Gbps Monolithic Optical Receiver with Avalanche Photodetector in 28nm CMOS

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Introduction

- The demand for high-bandwidth interconnects has led to the widespread adoption of optical interconnect solutions
- One cost-efficient solution is realizing PDs with the Si IC fabrication technology and integrating them with Si electronic
- This work presents the 20Gbps monolithic optical receiver designed with an equivalent circuit model of Si APD and under-damped TIA that compensates for the Si APD bandwidth limitation in the 28-nm process.

Avalanche Photodetector

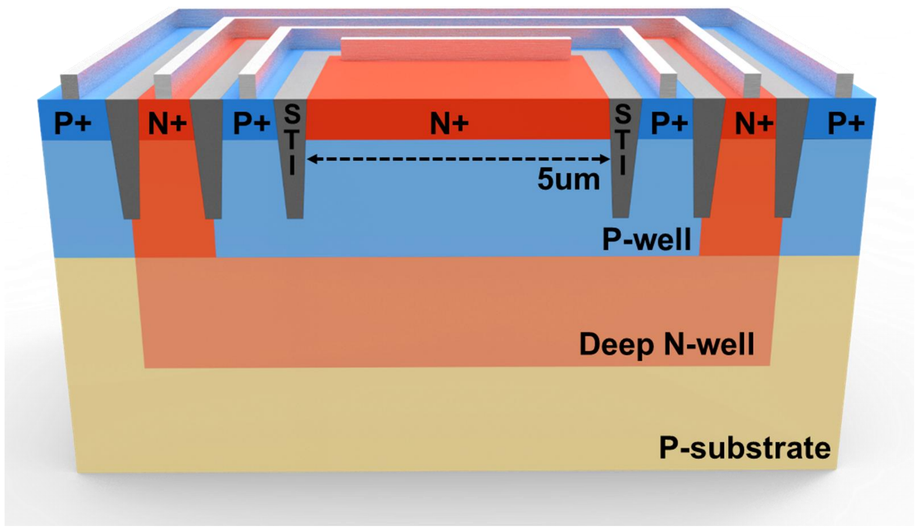
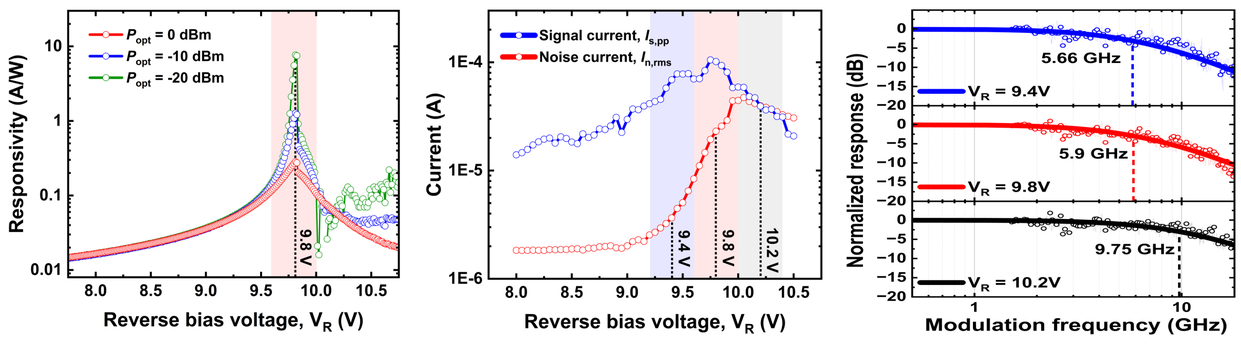
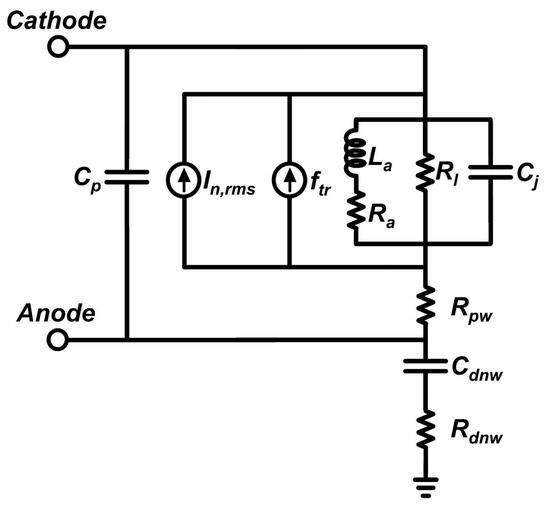


Fig 1. Cross-section of the N+/P-well Si APD in 28 nm CMOS

- The device relies on the vertical N+/P-well junction for photodetection.
- The N+/P-well structure is used because it can provide a larger photodetection bandwidth due to the larger minority carrier mobility than the P+/N-well junction





	9.4V	9.8V	10.2V
C_p (fF)	5		
L_a (nH)	20	14	4.3
R_a (Ω)	12800	825	240
R_l (kΩ)	20	12	8
C_j (fF)	19	16	12
R_{pw} (Ω)	100		
R_{dnw} (Ω)	220		
C_{dnw} (fF)	190	165	140
f_{tr} (GHz)	5.8	5.9	9
$I_{n,rms}$ (μA)	3.6	23	38.4

Fig 2. Measurement results of Si APD and the equivalent circuit model

- The responsivity, bandwidth, and noise current of the Si APD are measured and the corresponding equivalent circuit model is presented
- The reverse bias voltage of 9.4 V is chosen to design a monolithic optical receiver

Monolithic Optical Receiver

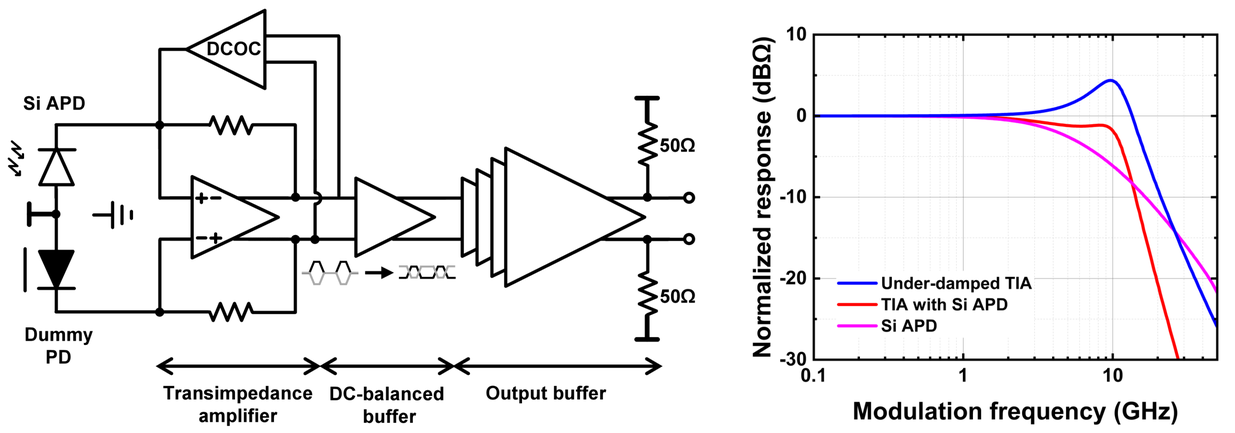


Fig 3. Block diagram of monolithic optical receiver and frequency response of the Si APD with under-damping TIA

- The monolithic optical receiver is composed of Si APD, under-damping TIA with DC offset cancellation, DC balanced buffer, and output buffer
- The under-damping TIA compensates the bandwidth limitation of Si APD

Measurement Results

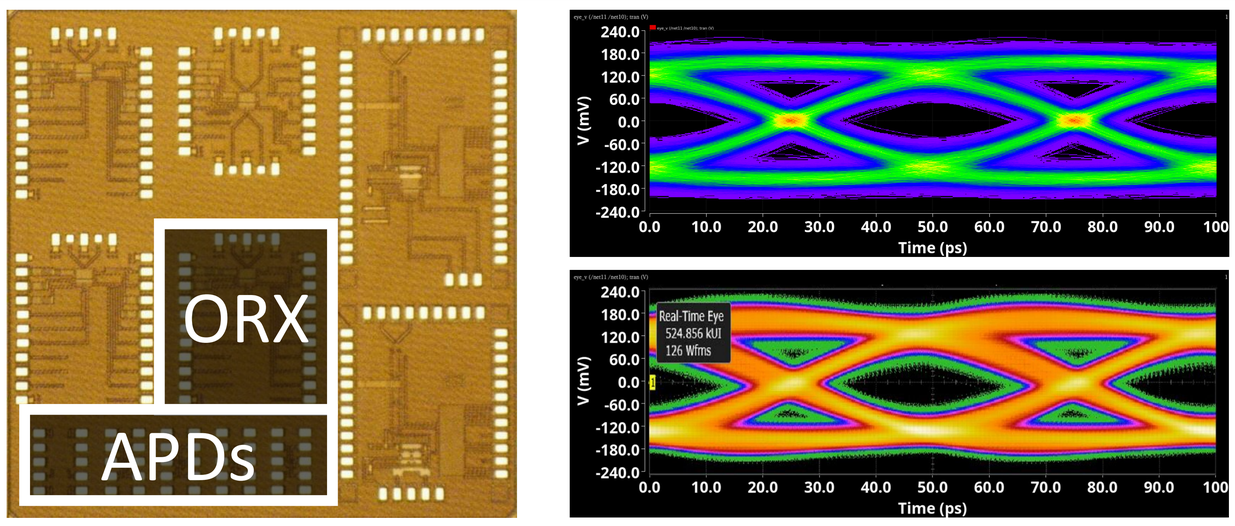


Fig 4. Chip photo with eye diagrams of simulation and measurement

	Optics Express 2012	*TCAS-I 2019*	*JSTQE 2016*	*This work JLT 2024*
Process	0.25 μm BiCMOS	0.13 μm CMOS	65 nm CMOS	28 nm CMOS
Data rate	12.5 Gb/s	10 Gb/s	18 Gb/s	20 Gb/s
PRBS	2^{31}-1	2^{7}-1	2^{15}-1	2^{31}-1
PD BW	5 GHz	3.5 GHz	1.1 GHz	5.66 GHz
PD responsivity	0.07 A/W	3.92 A/W	0.272 A/W	0.067 A/W
Sensitivity	-7 dBm	-18.8 dBm	-4.9 dBm	-4 dBm
Power*	59 mW	5.7 mW	48 mW	11.34 mW
Energy efficiency	4.72 pJ/b	0.57 pJ/b	2.7 pJ/b	0.567 pJ/b

* Excluding output buffer power

Fig 5. Comparison table of monolithic optical receiver

- Simulation with an equivalent circuit model shows good agreement with the measurement result
- BER under 10^{-12} has been achieved with 20Gbps PRBS31 data pattern, -4 dBm sensitivity and 0.567 pJ/b power efficiency

Conclusion

- The Si APD characteristics are measured and modeled with an equivalent circuit that accurately emulates Si APD frequency response and noise characteristics
- The highest 20Gbps monolithic 850 nm optical receiver realized with the standard 28nm CMOS technology without any process modification or design rule violation

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